A typical shape of the depletion regions of the two above noted junctions is illustrated in FIG. 1a where the source 14, the body region **13**, and the gate are connected to a reference potential GND (i.e., Vg=Vsub=Vs=0) and a certain VDS voltage (e.g., VDS=20V) is applied to the drain. Under these operating conditions, the junctions are inversely biased because of the applied VDS voltage, and the respective depletion regions extend into the drain well region down to a certain depth. By further incrementing the VDS voltage, as shown in FIG. 1b (e.g., VDS=25V where Vg=Vsub=Vs=0), the depletion regions of the junctions between the substrate and the drain well region **12** and between the drain well region and the body region **13** merge. This completely depletes the drain well region **12**, thus producing the desired RESURF condition.

A1

Please replace the paragraph beginning at page 4, line 16, with the following rewritten paragraphs:

FIG. 2a is a cross-sectional view illustrating a traditional LDMOS structure according to the prior art;

FIG. 2b is a cross-sectional view illustrating an LDMOS structure of the invention;

A2

Please replace the paragraph beginning at page 5, line 24, with the following rewritten paragraph:

The principles upon which the RESURF LDMOS structure of the invention are based will be better understood with reference to FIGS. 3a and 3b. The BV measurements illustrated in FIG. 3a were obtained with Vds=70V and Vg=Vs=Vsub=0V, and the PT measurements illustrated in FIG. 3b were obtained with Vds=Vg=Vs=70V and Vsub=0V. As shown in FIG. 3b, even if

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